

Claims 1-13 are pending.

The rejection of claims 1 – 4, 6, 8 – 10, 12, and 13 under 35 U.S.C. § 102(a) as anticipated by the Intel Server Chassis SBCE and its various components, and the rejection of claims 5, 7, and 11 under 35 U.S.C. § 103(a) as obvious over the Intel Server Chassis SBCE as applied to claims 1 and 8, and further in view of the I²C Specification (January 2000), are both respectfully traversed.

Applicant has filed a Petition for an Unintentionally Delayed Foreign Priority Claim to claim priority to Taiwanese Application Serial No. 092108198 (which published as Publication No. TW 224273 B1). A copy of the Petition, including an accompanying Supplemental Application Data Sheet identifying the Taiwanese application, is attached hereto for the Examiner's convenience. A certified copy of the Taiwanese application was previously submitted. The Taiwanese application was filed on April 10, 2003, well within one year of the September 9, 2003 filing date of the present application.

The examiner is again thanked for bringing Applicant's attention to the benefits of claiming foreign priority.

As a result of the claim for foreign priority, the priority date of the present application predates the Intel Server Chassis SBCE, the primary reference. Because the Intel Server Chassis SBCE is removed from consideration as a prior art reference, and the I²C Specification by itself fails to teach all claim limitations, claims 1-13 are neither anticipated nor obvious in light of the prior art.

In view of the foregoing remarks, Applicant submits that the claims are in condition for allowance. A Notice of Allowance is therefore respectfully requested.

Dated: June 27, 2006

Respectfully submitted,



Miles Yamanaka
Reg. No. 45,665

FULBRIGHT & JAWORSKI L.L.P
555 South Flower Street , 41st Floor
Los Angeles, CA 90071
(213) 892-9200 – Telephone
(213) 892-9494 – Facsimile

Attachment:

Copy of Petition for an Unintentionally Delayed Foreign Priority Claim, including
Supplemental Application Data Sheet